Notice of References Cited	Application/Control No. 09/927,204	Applicant(s)/Patent Under Reexamination FOLTIN ET AL.	
	Examiner Thomas H. Stevens	Art Unit 2123	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,023,568	02-2000	Segal, Russell B.	716/6
	B	US-6,453,436	09-2002	Rizzolo et al.	714/726
	C	US-6,158,022	12-2000	Avidan, Jacob	714/33
	D	US-5,933,356	08-1999	Rostoker et al.	703/15
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Kulshreshtha et al., "Transistor-level Timing Anaylsis using Embedded Simulation" IEEE 2000 pg. 344-349.
	V	Albrecht et al., " Cycle Time and Slack Optimization for VLSI-chips" pg.232-238 1999 IEEE/ACM International Conference on Computer-aided Design
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.